Freescale Semiconductor
Technical Data

Document Number: MW4IC2230
Rev. 5, 5/2006

Replaced by MW4IC2230NBR1(GNBR1). There are no form, fit or function changes with this part replacement. N suffix added to part number to indicate transition to lead-free terminations.

RF LDMOS Wideband Integrated Power Amplifiers

MW4IC2230MBR1
MW4IC2230GMBR1

2110-2170 MHz, 30 W, 28 V
SINGLE W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

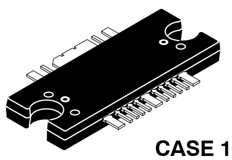
The MW4IC2230M wideband integrated circuit is designed for W-CDMA base station applications. It uses Freescale's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband on-chip design makes it usable from 1600 to 2400 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, CDMA and W-CDMA.

Final Application

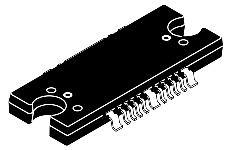
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 60 mA, I_{DQ2} = 350 mA, P_{out} = 5 Watts Avg., f = 2140 MHz, Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 31 dB
  Drain Efficiency — 15%
  ACPR @ 5 MHz = -45 dBc in 3.84 MHz Bandwidth

Driver Application

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 60 mA, I_{DQ2} = 350 mA, P_{out} = 0.4 Watts Avg., f = 2140 MHz, Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 31.5 dB
  ACPR @ 5 MHz = -53.5 dBc in 3.84 MHz Bandwidth
- Capable of Handling 3:1 VSWR, @ 28 Vdc, 2170 MHz, 5 Watts CW Output Power
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 10 mW to 5 W CW P_{out}.
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- 200°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel



CASE 1329-09
TO-272 WB-16
PLASTIC
MW4IC2230MBR1



CASE 1329A-03
TO-272 WB-16 GULL
PLASTIC
MW4IC2230GMBR1

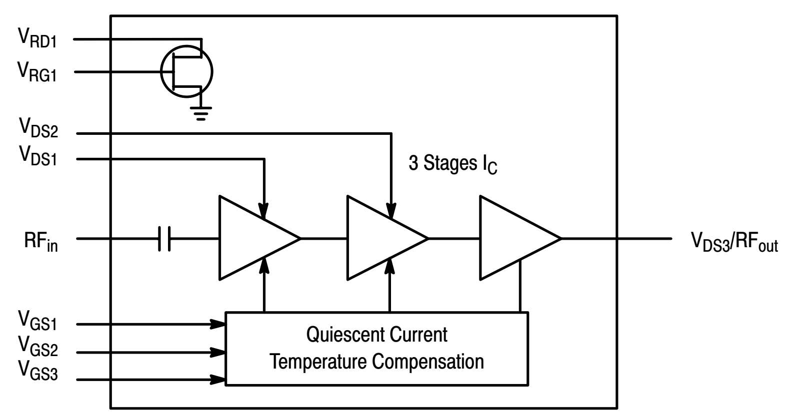
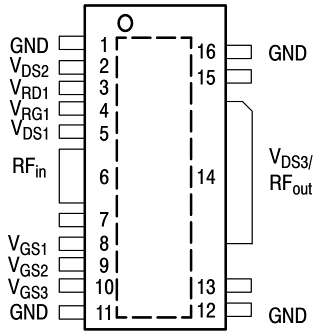


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside flag is source terminal for transistors.

Figure 2. Pin Connections

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1. Refer to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +8	Vdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Operating Channel Temperature	T_J	200	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [1]	Unit
Thermal Resistance, Junction to Case Stage 1 Stage 2 Stage 3	$R_{\theta JC}$	 10.5 5.1 2.3	°C/W

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C5 (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

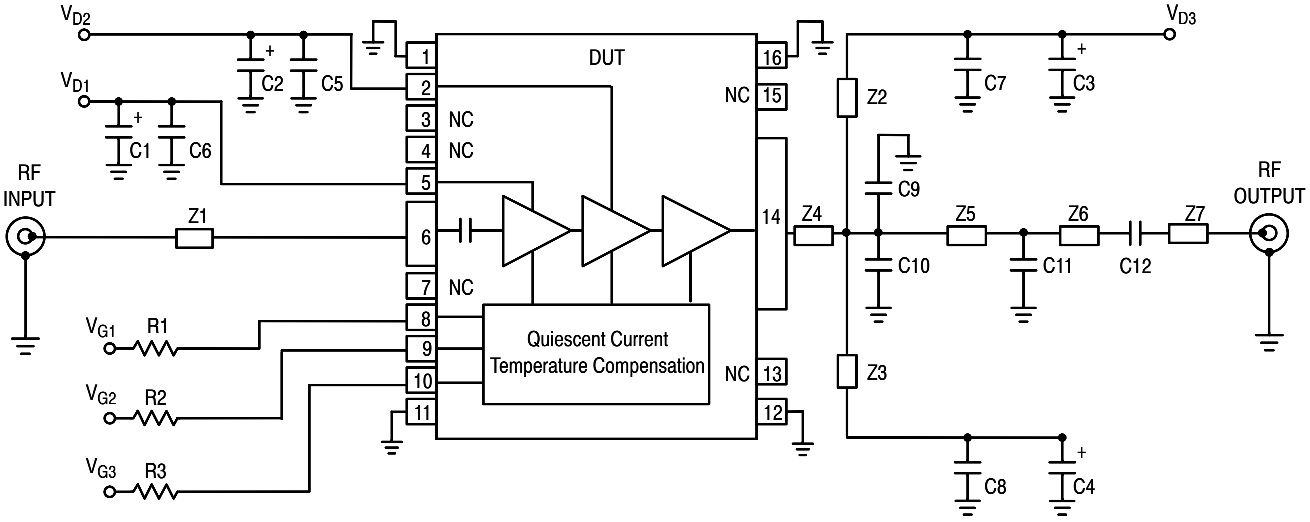
Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 60 mA, I_{DQ2} = 350 mA, I_{DQ3} = 265 mA, P_{out} = 0.4 W Avg., f = 2110 MHz, f = 2170 MHz, Single-carrier W-CDMA. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.					
Power Gain	G_{ps}	29	31.5	—	dB
Input Return Loss	IRL	—	-25	-10	dB
Adjacent Channel Power Ratio P_{out} = 0.4 W Avg. P_{out} = 1.26 W Avg.	ACPR	 — —	 -53.5 -52	 -50 —	dBc
Typical Performances (In Freescale Test Fixture tuned for 0.4 W Avg. W-CDMA driver) V_{DD} = 28 Vdc, I_{DQ1} = 60 mA, I_{DQ2} = 350 mA, I_{DQ3} = 265 mA, 2110 MHz<Frequency <2170 MHz					
Saturated Pulsed Output Power (f = 1 kHz, Duty Cycle 10%)	P_{sat}	—	43	—	W
Quiescent Current Accuracy over Temperature (-10 to 85°C) [2]	ΔI_{QT}	—	±5	—	%
Gain Flatness in 30 MHz Bandwidth	G_F	—	0.13	—	dB
Deviation from Linear Phase in 30 MHz Bandwidth	Φ	—	±1	—	°
Delay @ P_{out} = 0.4 W CW Including Output Matching	Delay	—	1.6	—	ns
Part-to-Part Phase Variation	$\Delta\Phi$	—	±15	—	°

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977.

(continued)

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Reference Application Circuit tuned for 2-carrier W-CDMA signal) V_{DD} = 28 Vdc, P_{out} = 0.4 W Avg., I_{DQ1} = 60 mA, I_{DQ2} = 400 mA, I_{DQ3} = 245 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz, 2-carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. IM3 measured in 3.84 MHz Channel Bandwidth @ ±10 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.					
Power Gain	G_{ps}	—	31.5	—	dB
Intermodulation Distortion	IM3	—	-52	—	dBc
Adjacent Channel Power Ratio	ACPR	—	-55	—	dBc
Input Return Loss	IRL	—	-26	—	dB

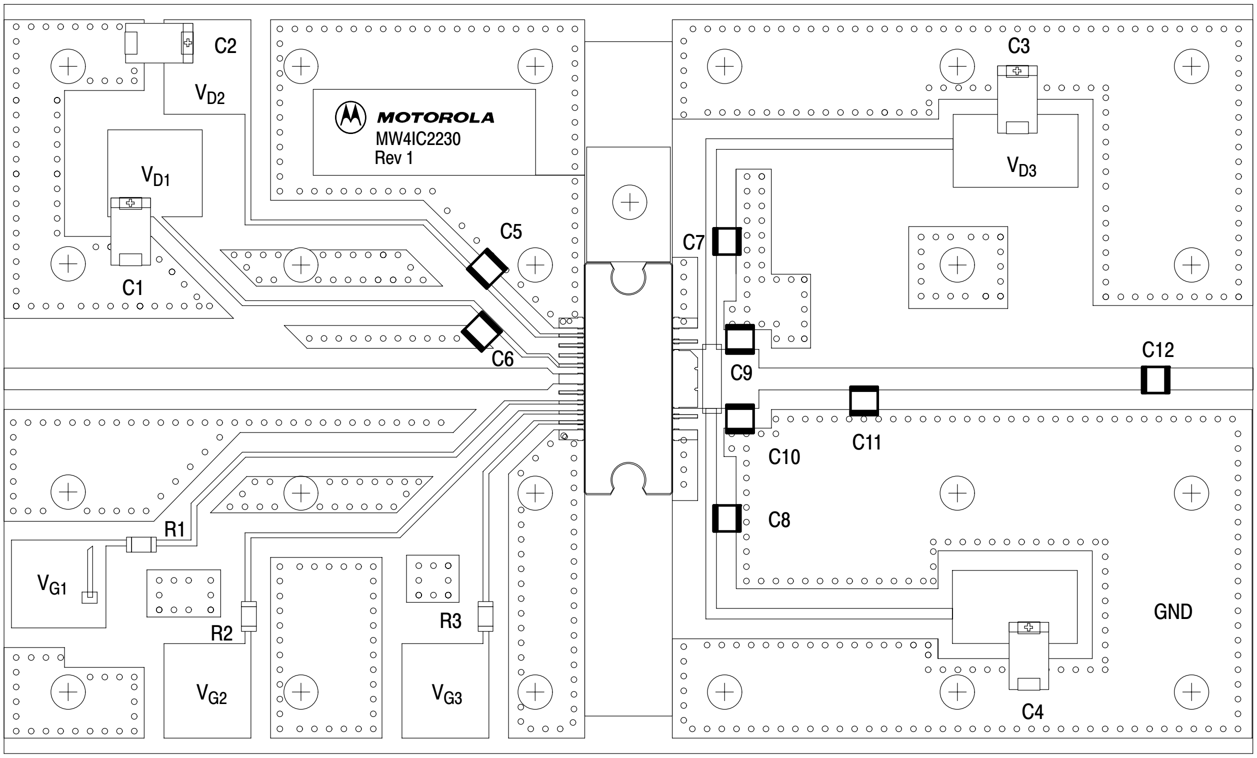


Z1	2.180″ x 0.090″ Microstrip	Z6	1.120″ x 0.090″ Microstrip
Z2, Z3	0.040″ x 0.430″ Microstrip	Z7	0.340″ x 0.090″ Microstrip
Z4	0.350″ x 0.240″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z5	0.420″ x 0.090″ Microstrip		

Figure 3. MW4IC2230MBR1(GMBR1) Test Circuit Schematic

Table 6. MW4IC2230MBR1(GMBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	10 μF, 35 V Tantalum Capacitors	TAJD106K035	AVX
C5, C6, C7, C8, C12	8.2 pF 100B Chip Capacitors	100B8R2CW	ATC
C9, C10	1.8 pF 100B Chip Capacitors	100B1R8BW	ATC
C11	0.3 pF 100B Chip Capacitor	100B0R3BW	ATC
R1, R2, R3	1.8 kΩ Chip Resistors (1206)		



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 4. MW4IC2230MBR1(GMBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

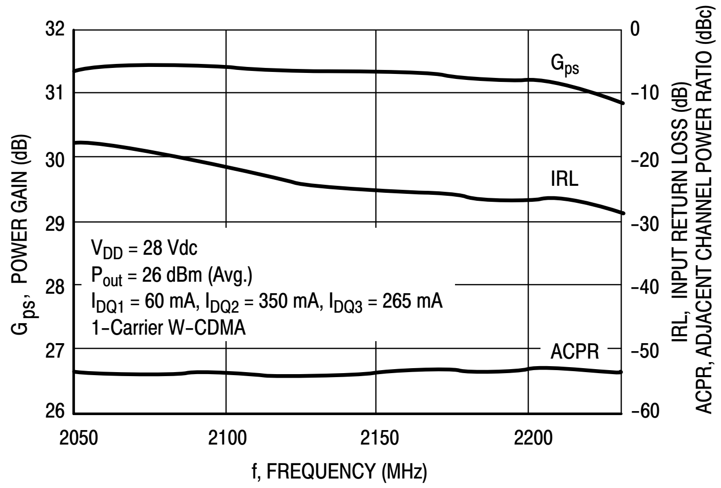


Figure 5. Single-Carrier W-CDMA Wideband Performance @ P_{out} = 26 dBm

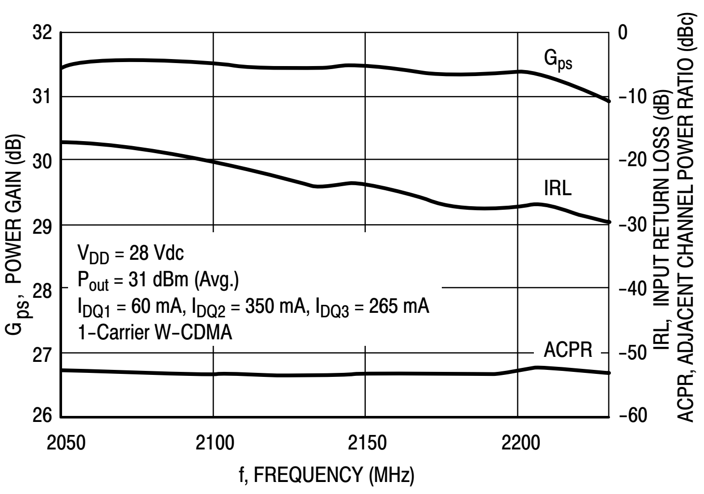


Figure 6. Single-Carrier W-CDMA Wideband Performance @ P_{out} = 31 dBm

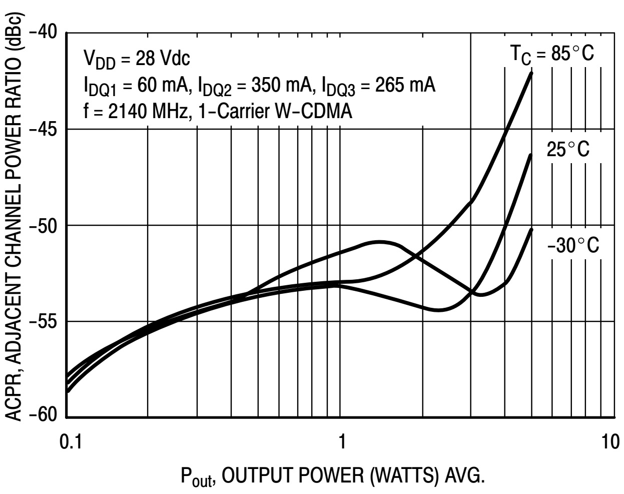


Figure 7. Adjacent Channel Power Ratio versus Output Power

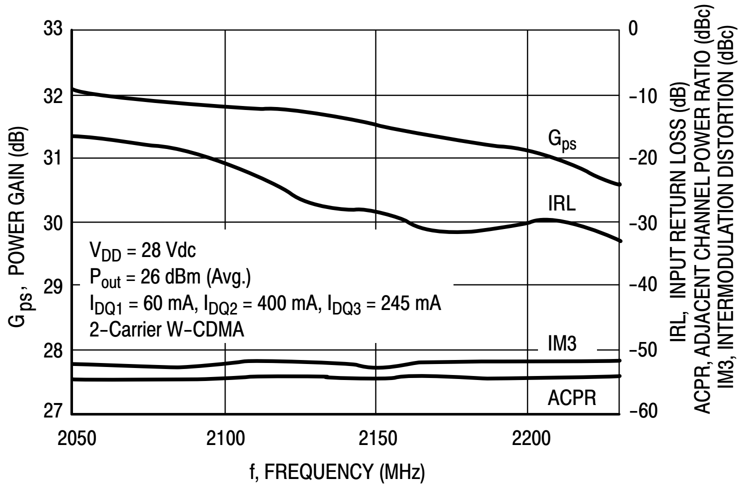


Figure 8. 2-Carrier W-CDMA Wideband Performance

TYPICAL CHARACTERISTICS

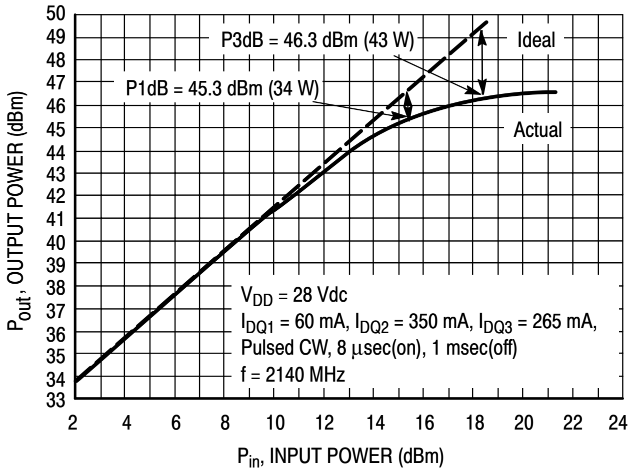


Figure 9. Output Power versus Input Power

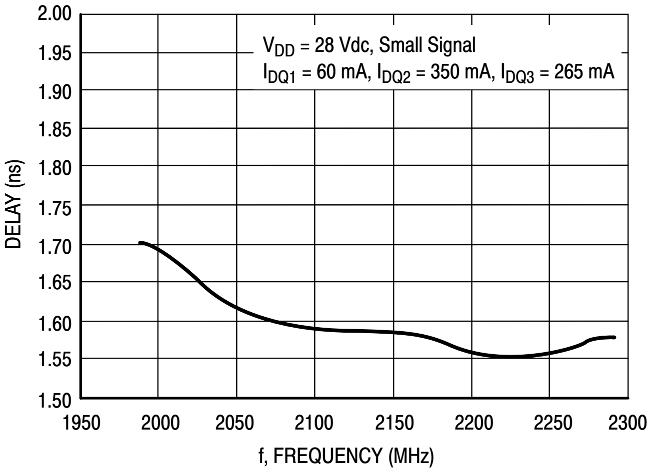
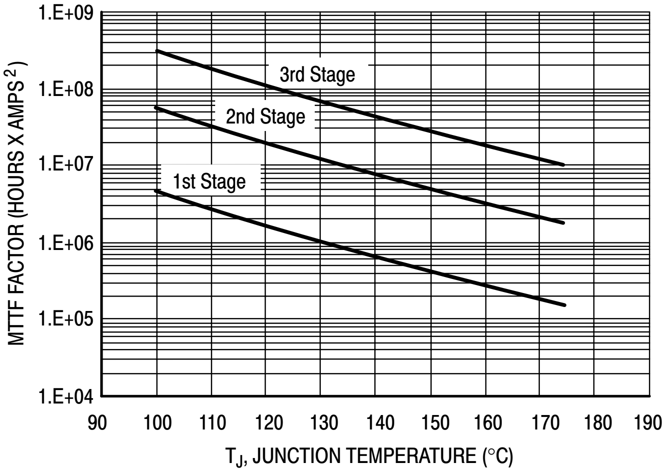
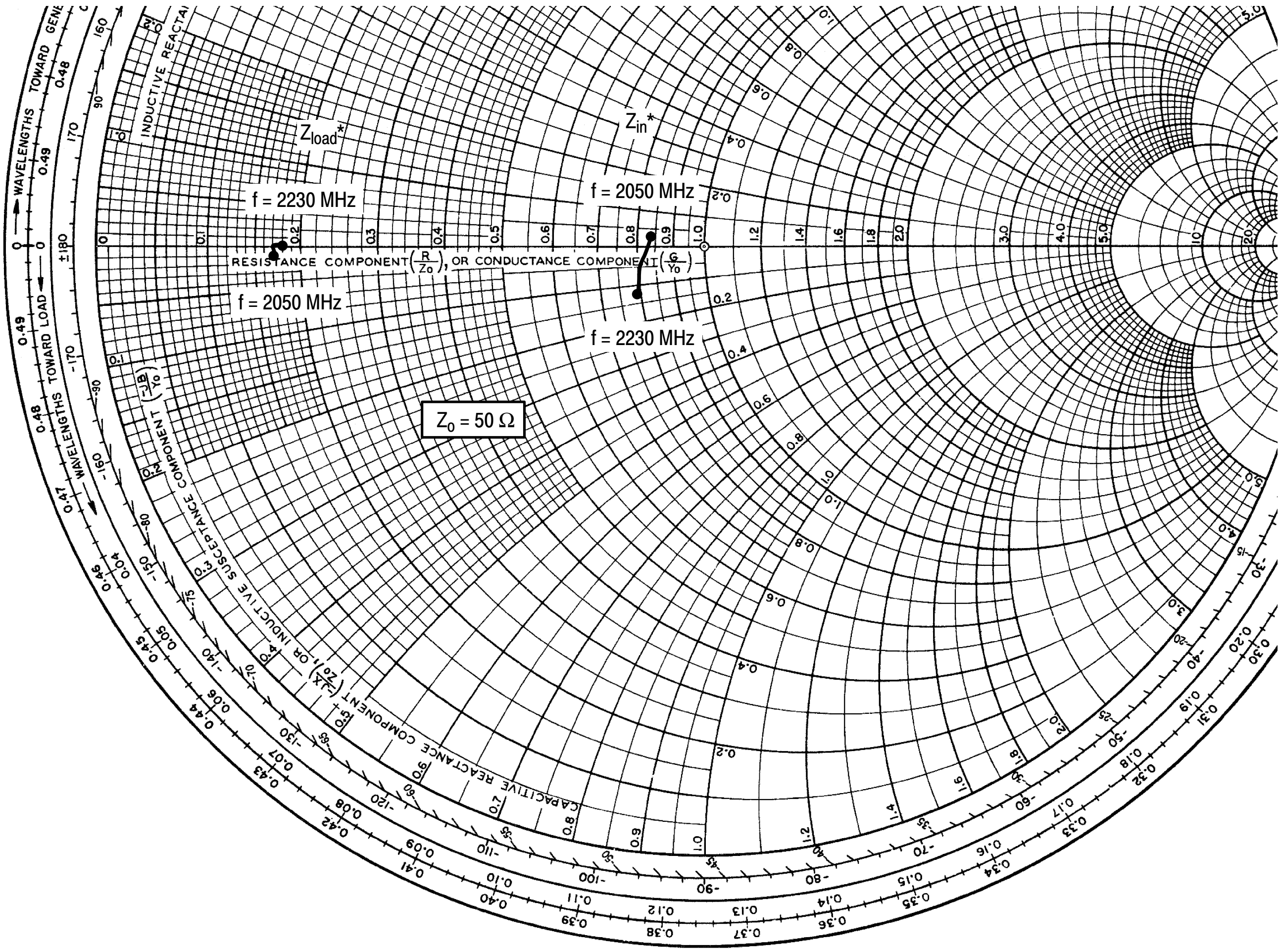


Figure 10. Delay versus Frequency



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 11. MTTF Factor versus Temperature Junction



V_{DD} = 28 V, I_{DQ1} = 60 mA, I_{DQ2} = 350 mA, I_{DQ3} = 265 mA, P_{out} = 26 dBm

f MHz	Z_{in} Ω	Z_{load} Ω
2050	42.18 + j1.49	8.52 - j0.46
2110	41.06 - j1.30	8.58 - j0.20
2140	40.49 - j2.42	8.63 - j0.09
2170	40.05 - j3.45	8.69 - j0.01
2230	39.29 - j6.31	8.81 + j0.04

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

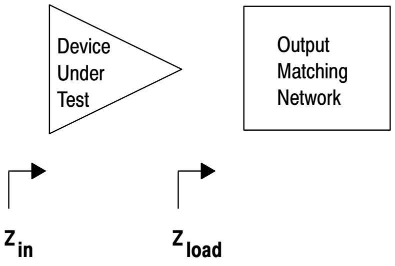
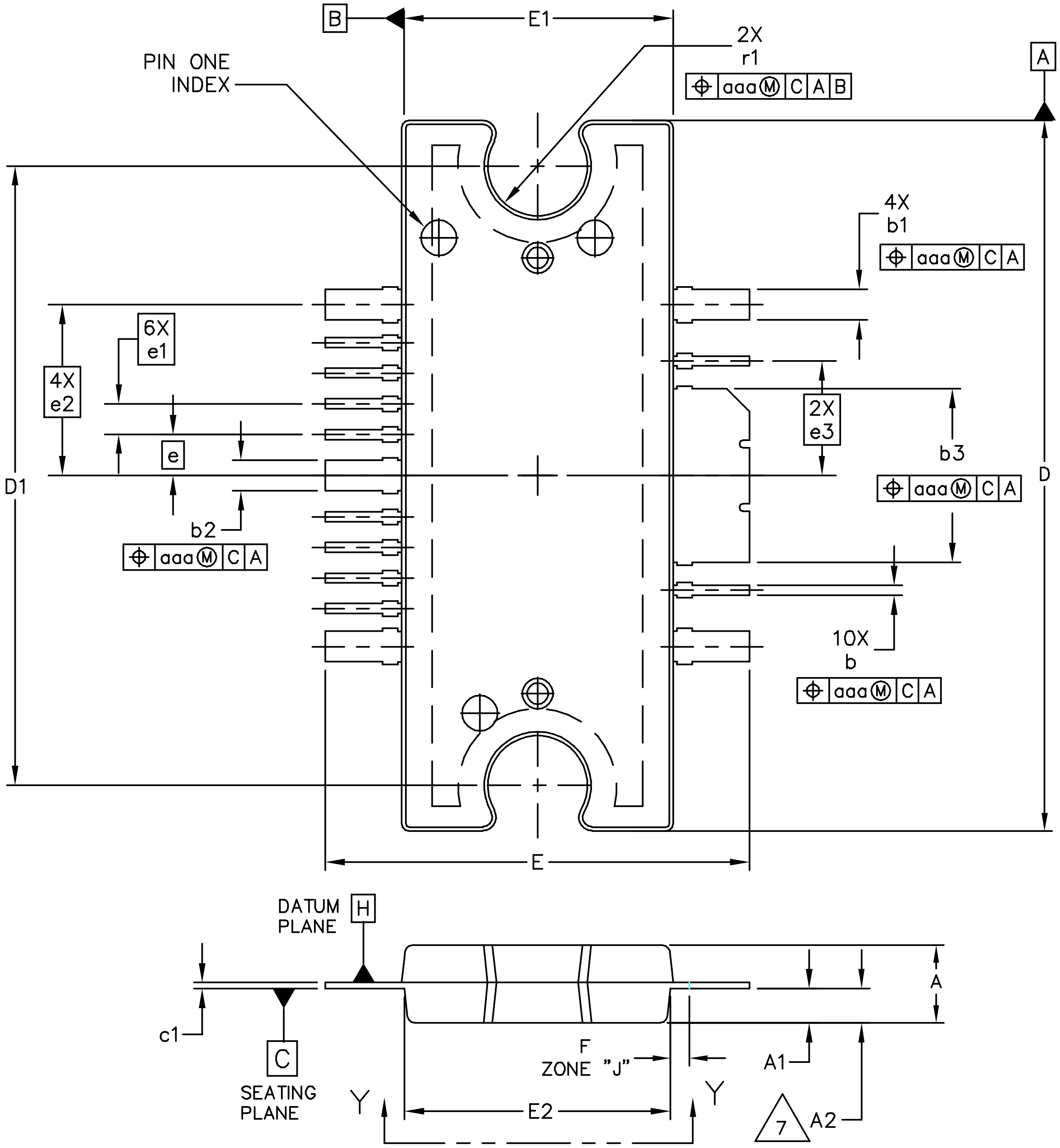


Figure 12. Series Equivalent Input and Load Impedance

NOTES

PACKAGE DIMENSIONS



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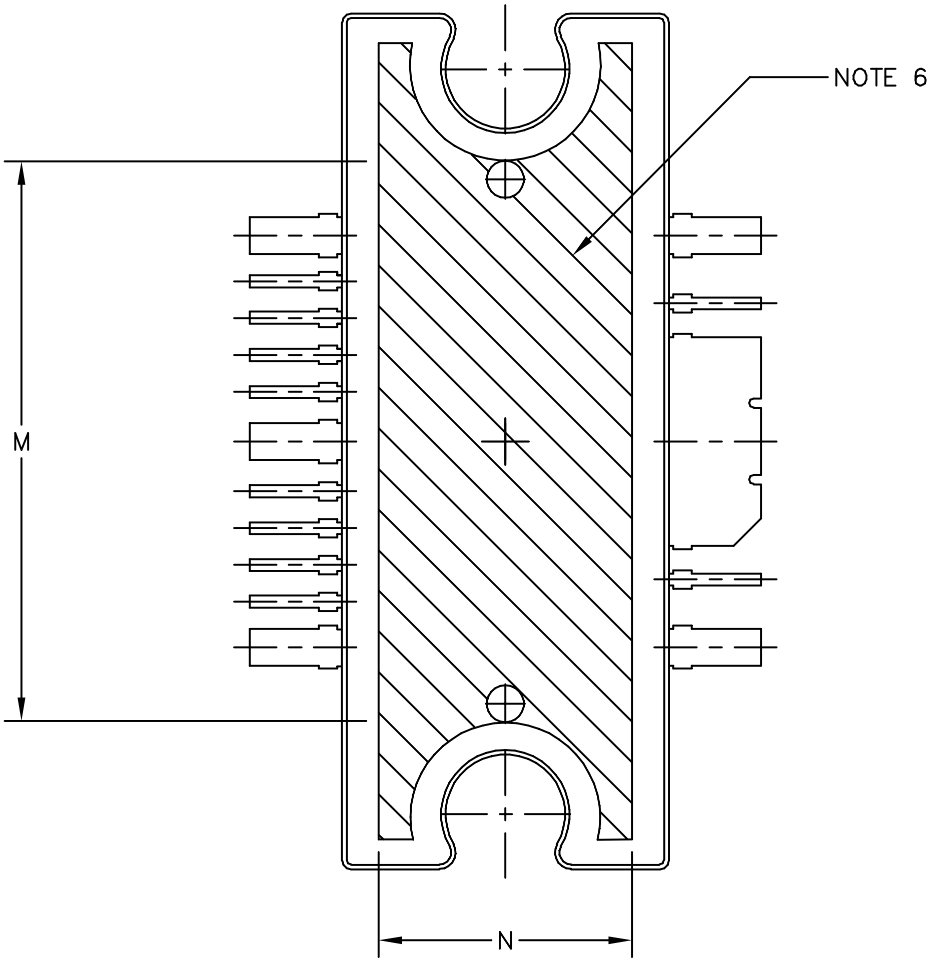
	CASE NUMBER: 1329–09	13 MAR 2006
	STANDARD: NON–JEDEC	



VIEW Y–Y

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	CASE NUMBER: 1329–09	13 MAR 2006
	STANDARD: NON–JEDEC	

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3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----					
					aaa	.004		.10	

MECHANICAL OUTLINE

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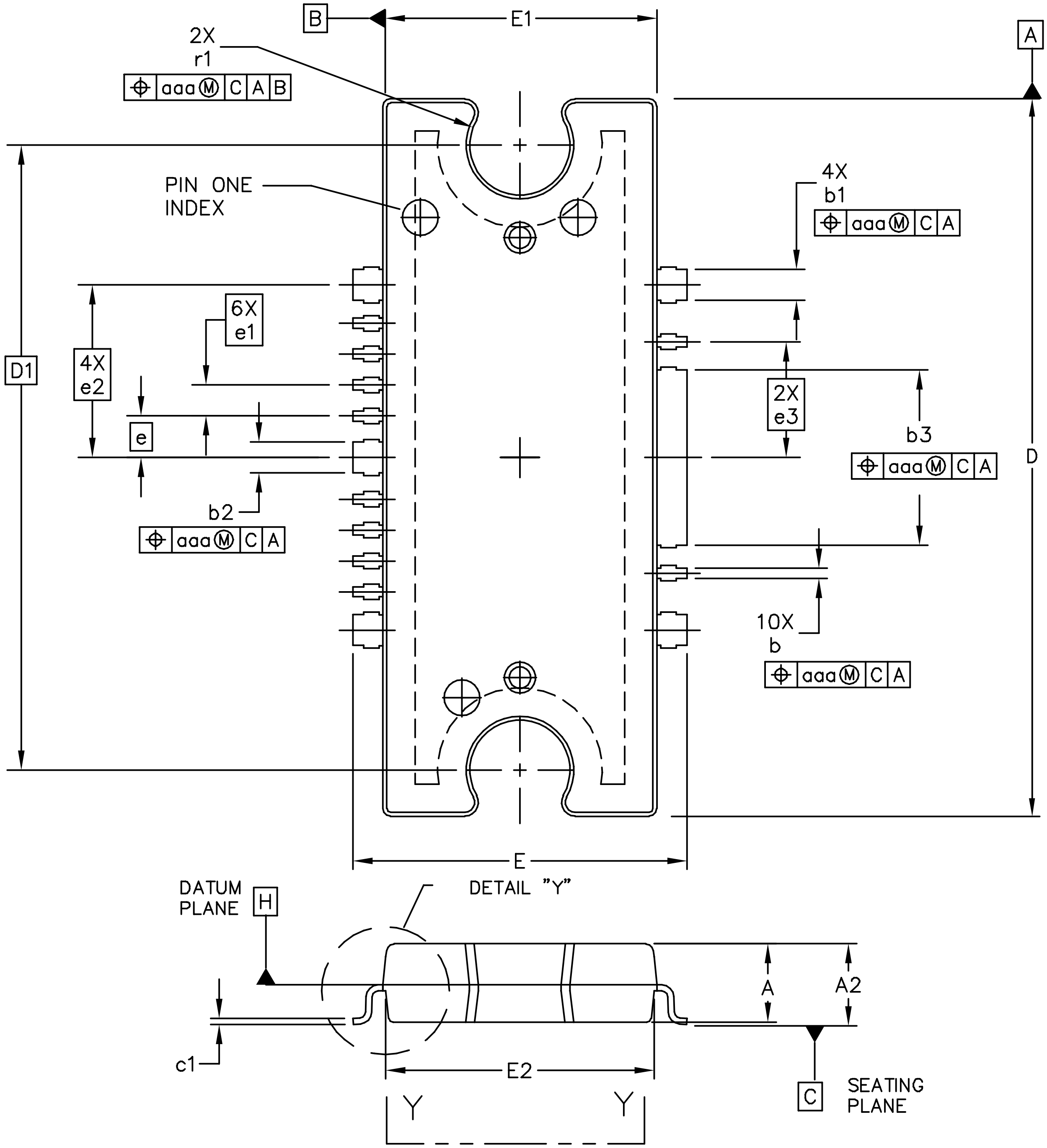

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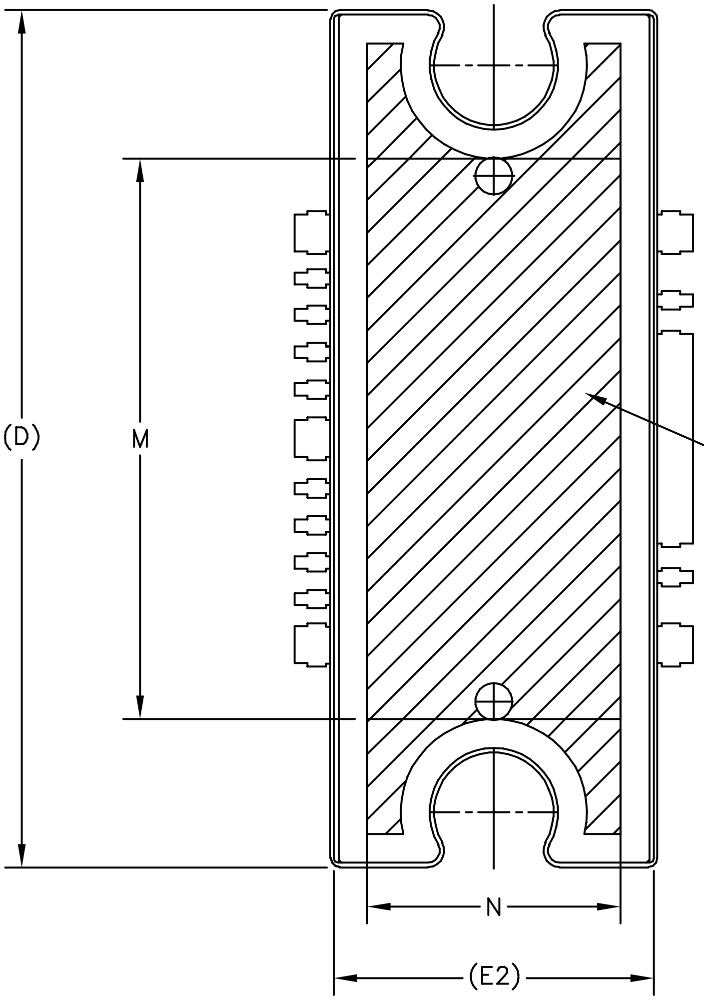

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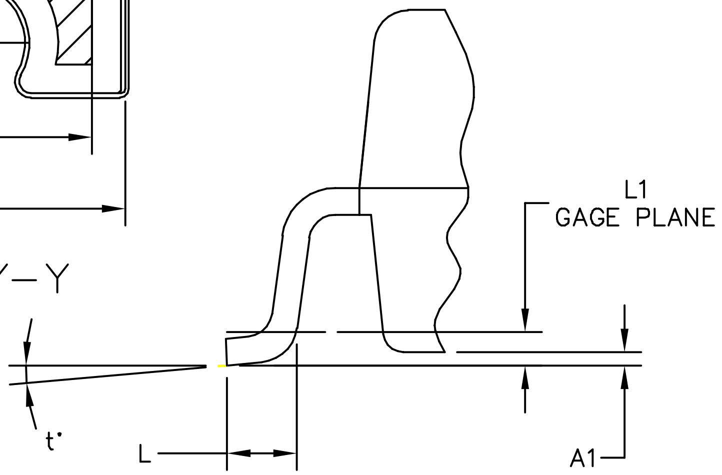

DETAIL "Y"

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	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.001	.004	0.02	0.10	b1	.037	.043	0.94	1.09
A2	.099	.110	2.51	2.79	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
L	.018	.024	4.90	5.06	e3	.150 BSC		3.81 BSC	
L1	.01 BSC		.025 BSC		r1	.063	.068	1.6	1.73
M	.600	----	15.24	----	t	2°	8°	2°	8°
N	.270	----	6.86						
				----	aaa	.004		.10	

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